

Refine Search

Search Results -

Term	Documents
(19 AND 7).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	1
(L19 AND L7).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	1

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L23

Refine Search

Recall Text

Clear

Interrupt

Search History

DATE: Tuesday, November 22, 2005 [Printable Copy](#) [Create Case](#)

<u>Set</u> <u>Name</u>	<u>Query</u>	<u>Hit</u> <u>Count</u>	<u>Set</u> <u>Name</u> result set
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L23</u>	l19 and l7	1	<u>L23</u>
<u>L22</u>	l19 and l6	4	<u>L22</u>
<u>L21</u>	l19 and l5	12	<u>L21</u>
<u>L20</u>	L19 and (instruction\$1 near4 cach\$3 or fill near3 buffer\$1)	12	<u>L20</u>
<u>L19</u>	L10 near35 (mux or multiplex\$5 or select\$5 or sel)	73	<u>L19</u>
<u>L18</u>	l11 and l7	1	<u>L18</u>
<u>L17</u>	l11 and l6	2	<u>L17</u>
<u>L16</u>	l11 and l5	9	<u>L16</u>
<u>L15</u>	l4 and l7	10	<u>L15</u>
<u>L14</u>	l4 and l6	5	<u>L14</u>
<u>L13</u>	l4 and l5	23	<u>L13</u>

<u>L12</u>	L11 and instruction\$1 near4 cach\$3	10	<u>L12</u>
<u>L11</u>	L10 and (mux or multiplex\$5 or select\$5 or sel) near12 configura\$6	34	<u>L11</u>
<u>L10</u>	L8 near35 (size or width or length)	485	<u>L10</u>
<u>L9</u>	L8 near35 (mux or multiplex\$5 or select\$5 or sel) near12 configura\$6	18	<u>L9</u>
<u>L8</u>	(plur\$7 or two or second) near5 (map\$6 or associat\$5) near8 (microinstruction\$1 or instruction\$1 or cod\$3)	16612	<u>L8</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L7</u>	(711/118-146)![CCLS]	7233	<u>L7</u>
<u>L6</u>	(712/212,213)[CCLS]	419	<u>L6</u>
<u>L5</u>	(712/2-300)[CCLS]	11598	<u>L5</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L4</u>	L3 and instruction\$1 near4 cach\$3	109	<u>L4</u>
<u>L3</u>	l2 and fill\$3 near4 buffer\$1	595	<u>L3</u>
<u>L2</u>	L1 and (mux or multiplex\$5 or select\$5 or sel) near12 configura\$6	8900	<u>L2</u>
<u>L1</u>	(map\$6 or associat\$5) near8 (microinstruction\$1 or instruction\$1 or cod\$3)	138460	<u>L1</u>

END OF SEARCH HISTORY



Welcome United States Patent and Trademark Office

Search Results **BROWSE** **SEARCH** **IEEE XPLORE GUIDE**

Results for "(((fill <near/6> (buffer) <and> map* <and> (size or width or length))<in>..."
Your search matched 1 of 1263585 documents.
A maximum of 100 results are displayed, 25 to a page, sorted by **Relevance** in **Descending** order.

[e-mail](#)

» Search Options

[View Session History](#)

[New Search](#)

Modify Search

☐ Check to search only within this results set

Display Format: ☒ Citation ☐ Citation & Abstract

» Key

- IEEE JNL IEEE Journal or Magazine
- IEEE JNL IEE Journal or Magazine
- IEEE CNF IEEE Conference Proceeding
- IEEE CNF IEE Conference Proceeding
- IEEE STD IEEE Standard

1. The direct-mapped instruction cache for ColdFire microprocessors
Tirumala, A.S.; Bibikar, V.J.;
Computer Design: VLSI in Computers and Processors, 1996. ICCD '96. Proceedings., 1996 IEEE I
Conference on
7-9 Oct. 1996 Page(s):288 - 292
Digital Object Identifier 10.1109/ICCD.1996.563569
[AbstractPlus](#) | Full Text: [PDF](#)(392 KB)

